Bandwidth Engine® MSR576 Board Design Guidelines

Application Note AN-603

Version 0.2, July 2012
MoSys, Inc.

Introduction

This application note describes board requirements and recommendations for use with the Bandwidth Engine MSR576. This document should be used in conjunction with Bandwidth Engine MSR576 Schematic Design Guidelines AN-606.

Requirements are items that must be met. Recommendations are guidelines, and the user should either adhere to these or to equivalent alternatives.

This document contains the following sections:

Definitions

Figure 1 Component overview

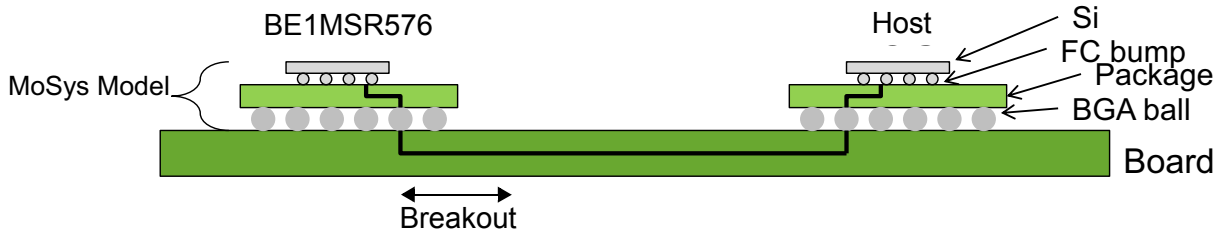


Table 1 Terminology

Term	Description
Bandwidth Engine (BE-1)	The MoSys™ device which is also known as MSR576.
Host	The ASIC, ASSP, or FPGA connecting to BE.
Flip Chip (FC or C4)	The bump connecting the chip to the package.
BGA (Ball Grid Array)	The solder ball connecting the package to the board.
Breakout	The routing region under the BGA and between BGA to the main board route. These routes may require special considerations such as thinner traces, plane voiding, via fields, etc. to escape out of the BGA field.
MoSys Package Model	Will include chip pad/Flip Chip bump to BGA/PCB interface.

Reference Design Kit

A reference board schematic and layout are available. These can be used as starting points.

- Characaterization Board schematic example (available as PDF file and ORCAD file)
- Characterization Board layout example, corresponding to a 20 layer board (*.brd)

Board Layout Requirements and Recommendations

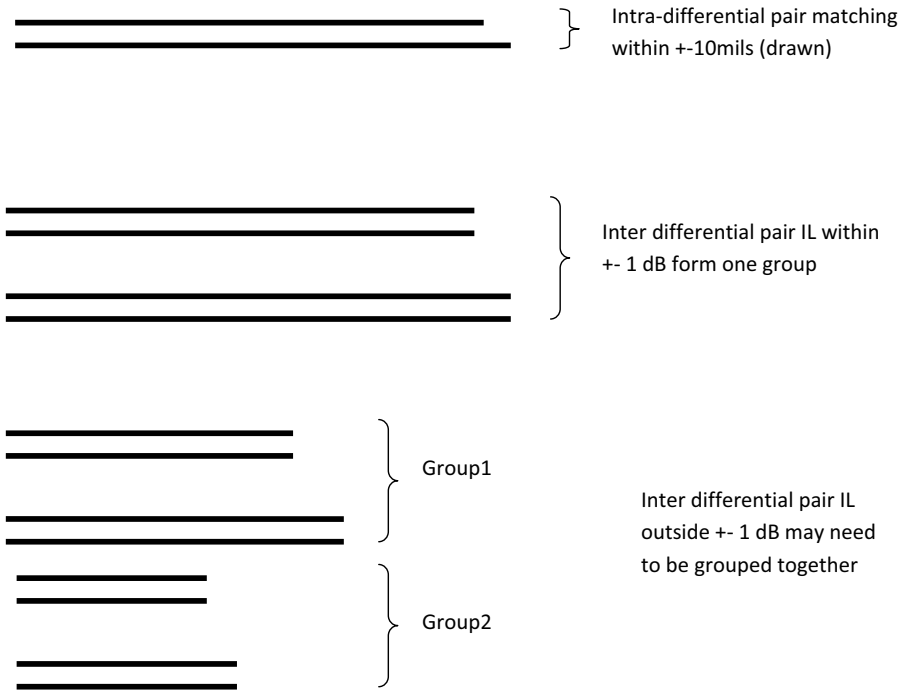
Signal Layout

For high speed signal layout striplines or microstrips can be used. Striplines are preferred because they have lower crosstalk, better impedance control, and lower EMI. Microstrips can be used provided overall interconnect criteria are met.

Routing signals on separate layers is acceptable, provided impedance, reflection, and crosstalk criteria are met.

Board loss requirements are shown in Table 2.

Figure 2 Matching requirements for the board interconnect. Grouping by IL may be required for optimum equalization purposes.



Reference Clock and Miscellaneous Signal Routing

Use the following guidelines for reference clock and miscellaneous signal routing:

Reference Clock

- The reference clock should be routed as a differential pair, with a differential impedance of 100 Ω +/- 10%.
- Isolation of -60 dB to any other signal is recommended.

Miscellaneous Signals

- Miscellaneous signals that must be routed as 50 Ω are EVENTA#, EVENTB#, SPI_SS#, SPI_SDO, SPI_SDI, SPI_SCLK. It is recommended that the EVENT pins be routed on as short a trace as possible back to the controller. The trace delay for the EVENT signals needs to be no more than 2.5 to 3.0ns.
- Miscellaneous signals RESET#, CONFIG#, CLKDIVIDE, are static and do not need to be routed as 50 Ω. READY# is a very slow switching signal and does not need to be routed as 50 Ω.

The reference for both of the above should be ground.

Spare Pins Routing Recommendation

Note the following recommendations for routing spare pins:

- There are 4 sets of differential pairs that are “spare”, and not used in MSR576.
- Routing these spares is primarily a customer board usage roadmap.
- MoSys recommends that the spare traces be drawn like actual high frequency traces, and characterized as such. This will permit compatibility with future Bandwidth Engine devices, which might use more lanes.
- It is optional that the spare traces are tied to ground using a 1 kΩ resistor to prevent a floating trace. This can be done at one end of the line by placing a resistor from the pad to the nearest ground. If the traces are active using a future generation component, these resistors should be removed. For new boards actively using the spare lanes, these resistors should not be placed.

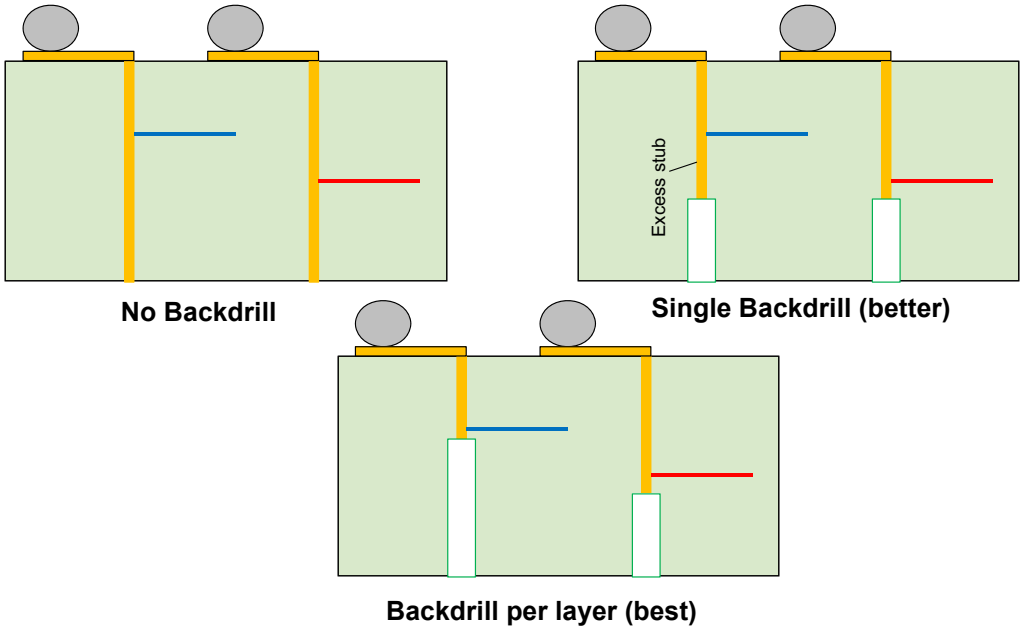
Backdrill Recommendation

The following are backdrill recommendations:

- Backdrill may be required to meet the return and insertion loss of Table 2.
- Backdrill to within 10 mils of signal layer is recommended.
- Backdrill per signal layer may be required, keeping the stub within 10 mils. This is the best and recommended option.

See Figure 3 for backdrilling options.

Figure 3 Backdrill recommendation

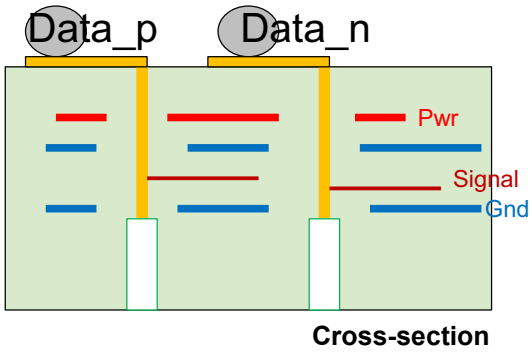


Via Recommendation

Vias need to form a 50 Ω impedance Tline. Some knobs:

- May require voiding of Pwr/Gnd plane directly under the BGA pad.
- Via placement (diff pair) are typically at the same pitch as BGA, 1mm.
- Via diameter: ~10-14 mil diameter
- Anti-pad sizing: ~30-35 mil diameter
- Usually a design may have more Vss planes, relative to the number of power planes. In such a case, the ground anti-pad can be larger than the power plane.
- Consult the layout in the design kit for a detailed example.

Figure 4 Via recommendation

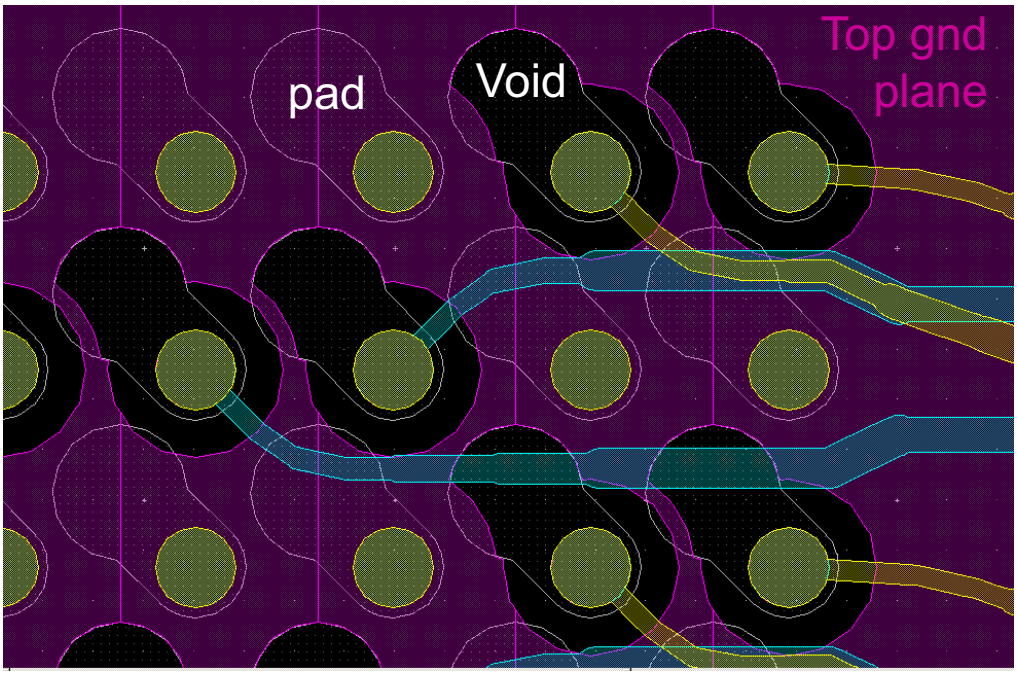


Ground Void Recommendation

BGA pads should be as small as manufacturing permits to help reduce excess capacitance. The Ground/Power directly under the pad may be voided as shown in Figure 5. This voiding reduces vertical capacitance between the BGA pad and the ground plane(s). If required, the top few planes may be voided.

Note: Usually an anti-pad may be in the same layer as a pad. It is the gap between the pad metal and the plane in the same layer. Void is a hole in the plane, with the idea of reducing vertical capacitance.

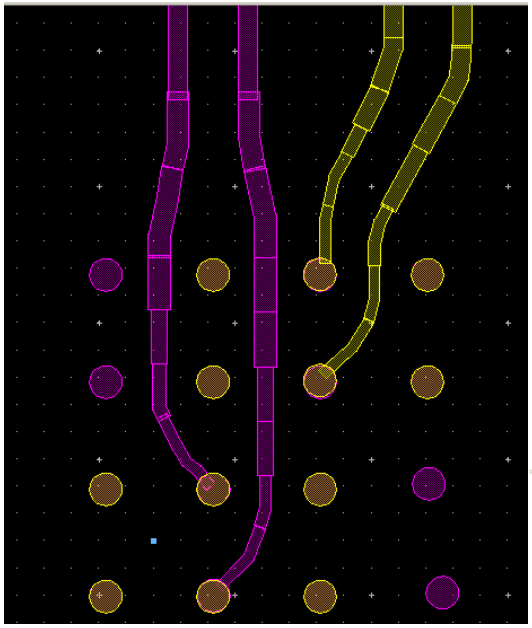
Figure 5 Ground void to reduce capacitance between BGA pad and ground.



BGA Escape Pattern

A BGA escape pattern example is shown in Figure 6. The characteristics of the breakout are highly dependent on pad, drill size, and board stackup, and need to be customized. See the example layout in the design kit.

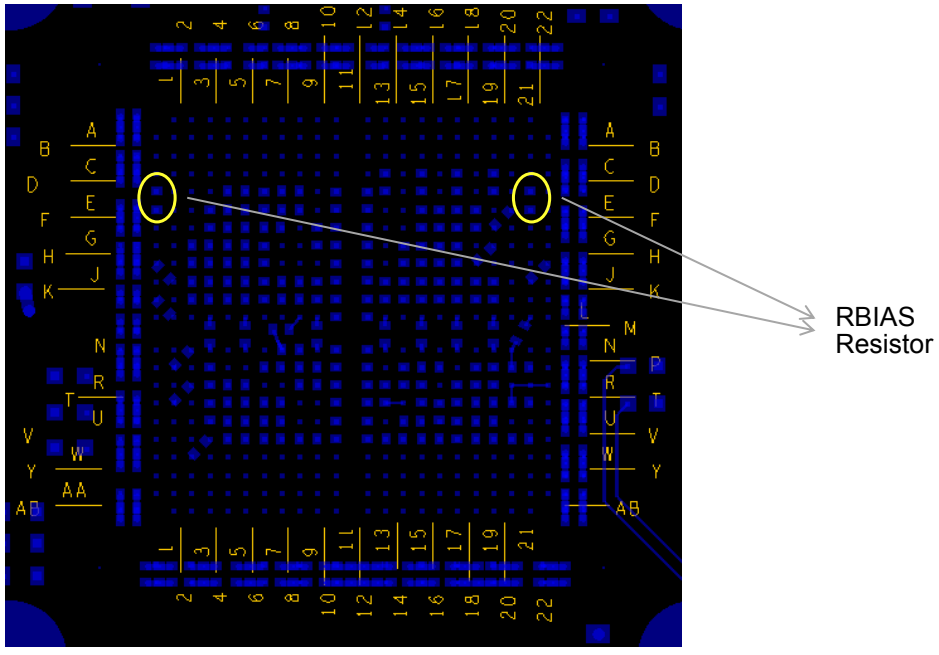
Figure 6 Example of a BGA escape pattern



Bias Resistor Placement Requirement

It is recommended that the bias resistor be placed directly underneath the component between the resistor and its sense pin as show in Figure 7. The capacitance (board trace, and pad) must be < 2pF.

Figure 7 Bias resistor placement under the component



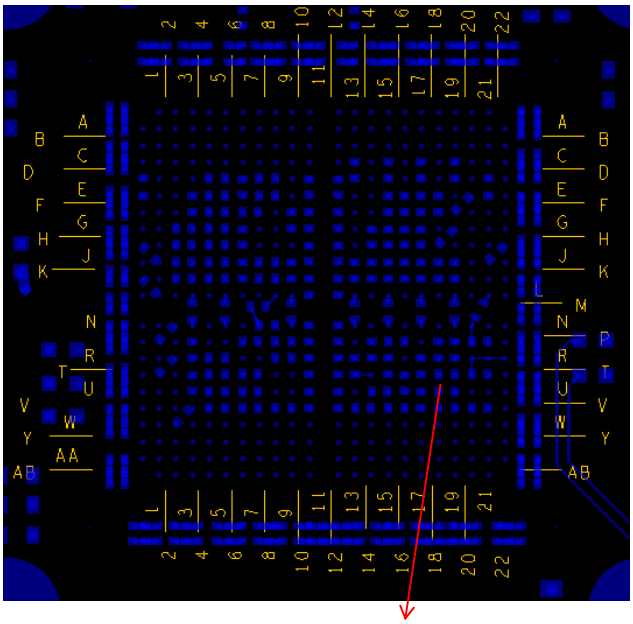
Power Routing Guidelines

- Place VDD and VSS vias adjacent as a pair. Add as many VDD-VSS core via pairs as required.
- Use planes for all power supplies.
- Recommend using the top most (or towards the top) plane for VDDA_SDS supply which will lower loop inductance.
- Populate decap under the component for most VDD and VSS balls adjacent as a pair.

MSR576 Decap Placement Recommendation

Figure 8 shows recommendations for MSR576 decap placement.

Figure 8 MSR576 decap placement recommendation



Board Design and Verification Requirements and Recommendations

Customer Board Specific Requirements

Measurement Setup Model

The measurement setup defines measurement points and insertion and return loss, whether they are from

- Extracted models of boards and packages
- Compilation of cascaded models (extracted or measured)

- Measurement setup

The interconnect setup should include package and board along with associated parasitics. A soldered component is required for this application. If a socket is required in debug applications, it should be modeled (see Figure 11). Normal applications will use soldered parts.

Package models from vendors will be required to build this channel model. If no vendor package is available, then a reasonable package should be substituted in the interim. However, for final tapeout, the actual package models are required.

All SerDes signals must be referenced to a common ground. This is important as all the return paths are completed using Vss in the package.

The highest operating data rate of the links is 10.3125 Gbps. This corresponds to a Nyquist frequency of 5.15 GHz. For return loss, a corner frequency of ¾ x baud rate is also defined, as 7.73 GHz.

Figure 9 Setup of board for insertion and return loss characterization.

Loss Requirements

Table 2 Loss requirements of board

Parameter	Description
Insertion Loss	< -8 dB @ 5.15 GHz • Insertion Loss should be smooth, with +/- 0.5 dB variation ripple from DC to 7.73 GHz • Target impedance, Zo: 100 Ω +/-10% differential
Return Loss	< -12 dB from DC to 7.73 GHz including manufacturing tolerances
Crosstalk	< -36 dB @ 5.15 GHz (between nearest differential pair)
Intra-differential pair	To be matched within +/-10 mils (drawn). Required to keep differential pair close to 180 degrees out of phase.
Inter-differential interconnect	Match interconnect length within +/-1 dB. Otherwise, interconnect should be split into multiple groups, with each group matched within +-1 dB.

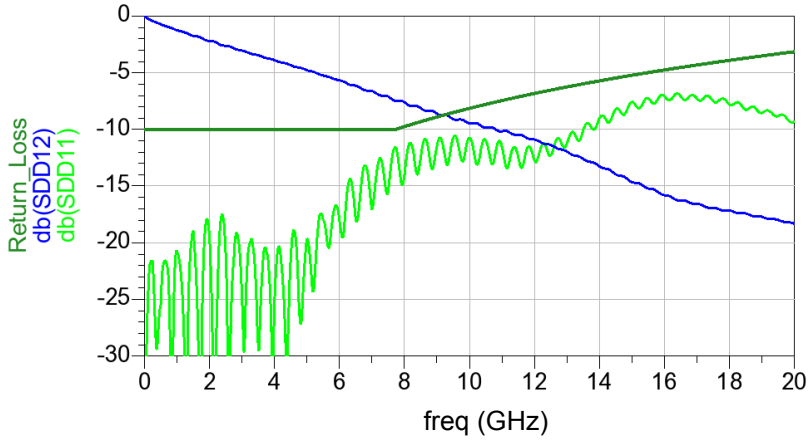
Figure 10 Board and package setup for insertion and return loss characterization

Table 3 Loss requirements with two packages and board

Parameter	Description
Insertion Loss	< -10 dB @ 5.15 GHz • Insertion Loss should be smooth, with +/- 0.5 dB variation ripple from DC to 7.73 GHz • Target impedance, Zo: 100 Ω +/-10% differential
Return Loss	< -10 dB from DC to 7.73 GHz including manufacturing tolerances
Crosstalk	< -36 dB @ 5.15 GHz (between nearest differential pair)
Intra-differential pair	To be matched within +/-10 mils (drawn on the board). Required to keep differential pair close to 180 degrees out of phase. The package should not introduce more than +/-2 mils (+/-50μm) additional skew.
Inter-differential skew	See next section for recommendation.

Figure 11 Packages, socket, and board setup for debug applications, and should meet requirements in Table 3.

Figure 12 Example of insertion and return loss. Configuration should meet the requirements in Table 3.



In addition to S-parameter measurements, it is highly desirable to perform a TDR analysis of impedance versus time (or length) as shown in Figure 12. This will identify any major discontinuities.

Figure 13 TDR setup to simulate board impedance profile.

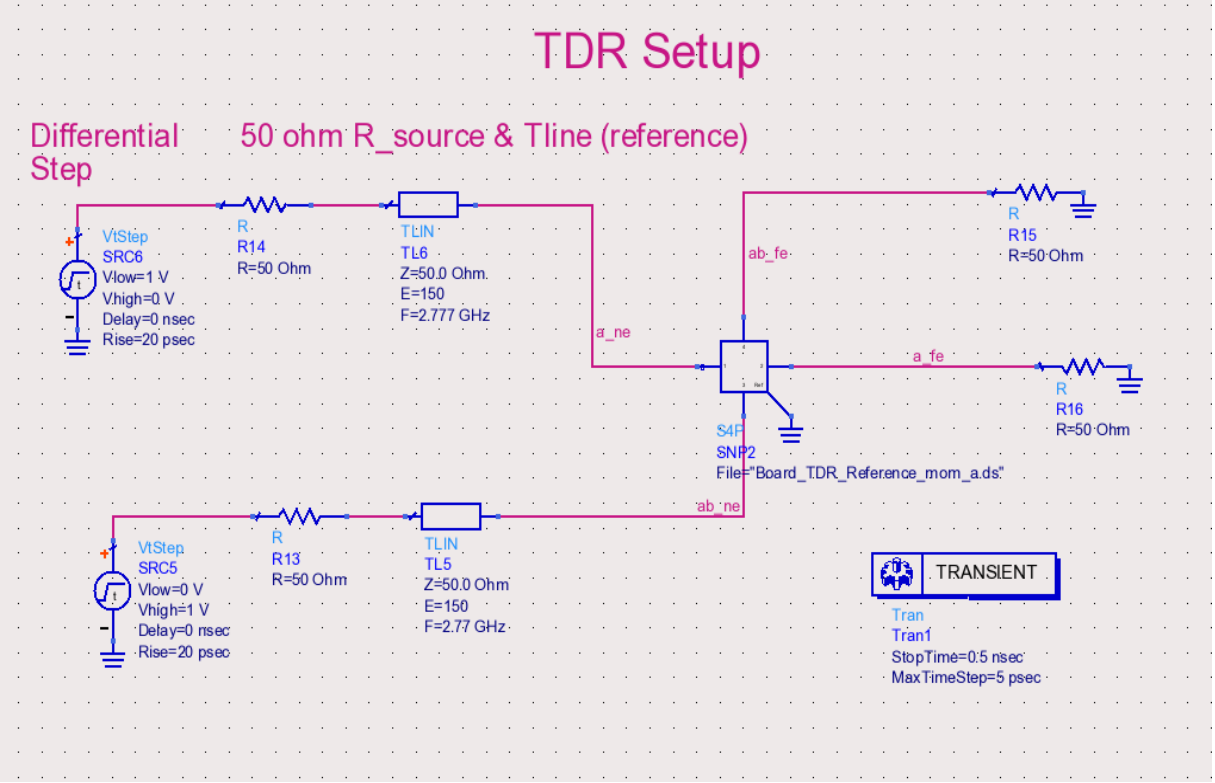
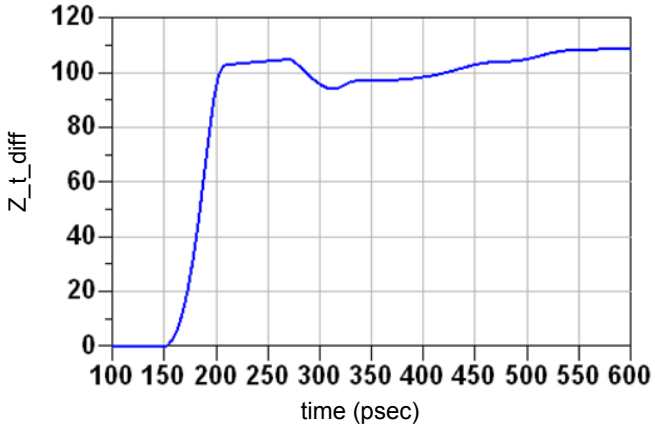


Figure 14 Example of TDR response



Board Design Recommendations

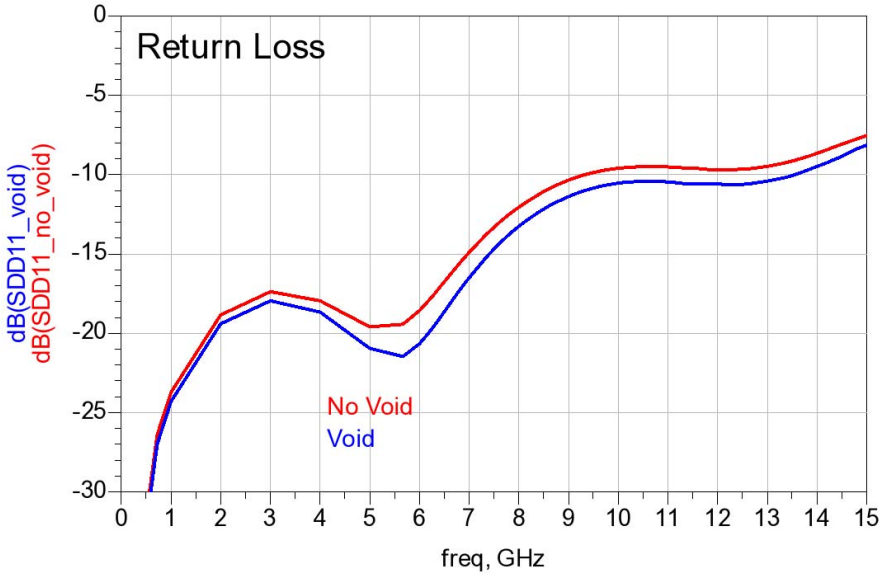
Following are board recommendations:

- GCI permits a range of interconnect skew that are leveled within the component. However, this also causes variable insertion loss. The overall equalization programming strategy is that available link margins should be simulated, and the allowable mismatch in insertion loss estimated. For example, when the link margins are smaller, the

insertion loss of the link should be matched tightly, or each lane should be programmed. However, if there is sufficient link margin, more interconnect loss skew may be acceptable, or coarser equalizer programming is acceptable.

- Make interconnect length matching within +/-1 dB. Otherwise, interconnect should be split into multiple groups, with each group staying within +-1 dB. Each group may need to be optimized for equalization if the channel is near its limits.
- Insertion loss should be smooth with +/-1 dB variation ripple from 7.73 GHz to 15.45 GHz (3/4 to 1 1/2 times the bit rate).
- The board must minimize discontinuities, in the form of excess capacitance or inductance, that cause large deviations from Zo.
- Back drilling of thicker boards is recommended to meet return loss.
- Use ground voids to reduce capacitance between BGA and ground and resulting return loss, as shown in Figure 15.

Figure 15 Ground void reduces return loss.

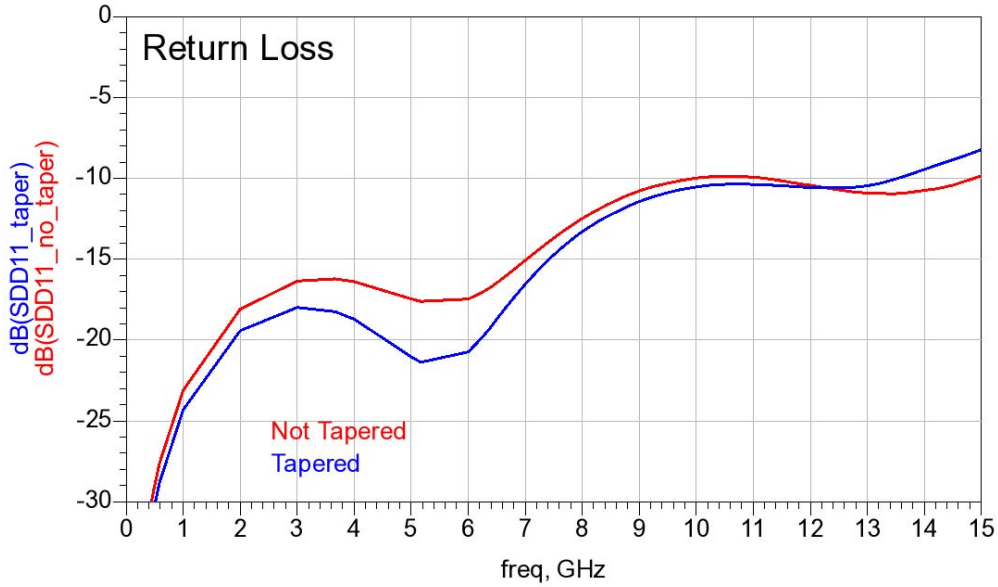


Example of a BGA Escape Pattern

Note the following with respect to the return loss shown in Figure 15 for the BGA escape pattern example in Figure 6:

- Return loss from vias and break out should be carefully extracted using a tool that comprehends 3D vias and ground return paths.
- A good target is < -20 dB in the frequency range DC to 5.15 GHz.
- The breakout is highly dependent on pad, drill size, and board stackup, and needs to be customized. See the example layout in the design kit. This can be adapted and extracted for the particular board stackup.

Figure 16 Return loss for a tapered BGA escape pattern



Board Power Requirements and Recommendations

Power Integrity Guidelines

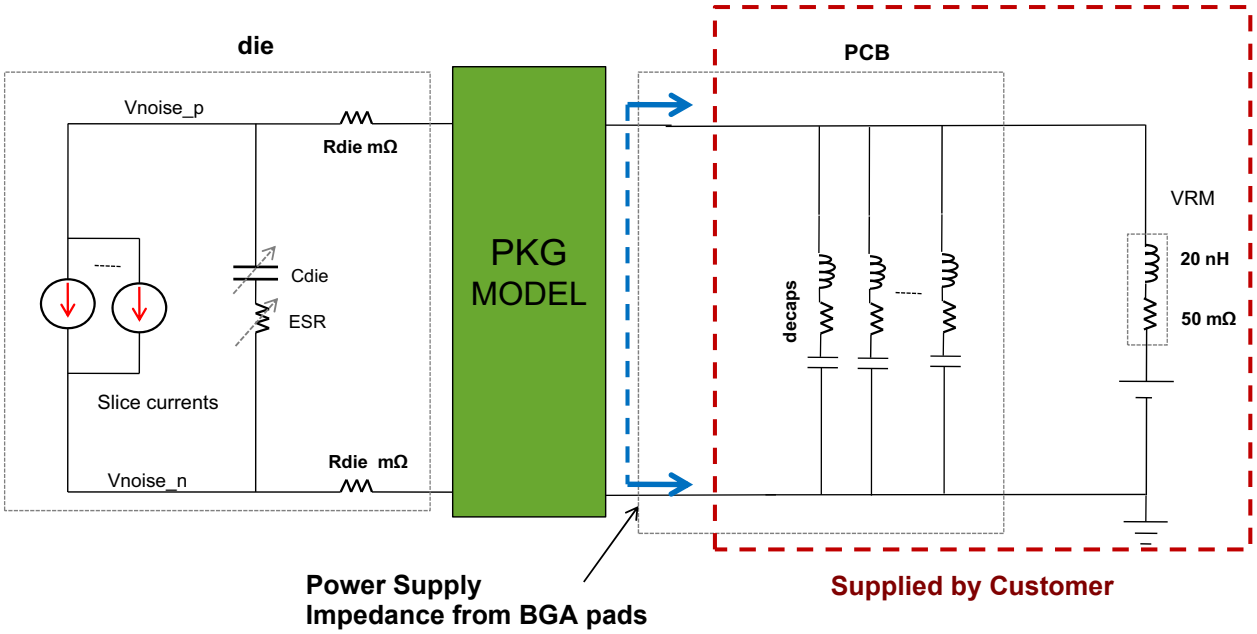
The VDDA_SDS (SerDes analog power supply) power supply has a tight voltage tolerance, and care must be taken to reduce loop inductance in the board.

Loop inductance can be reduced by following the routing guidelines in , “Power Routing Guidelines,” on page 7

Typical Test Bench for the Power Model

Figure 17 shows a typical test bench for the power model.

Figure 17 Typical test bench for the power model



VRM parasitic provided are representative values. For actual values consult your VRM vendor.

Power Sharing and Delivery

See MSR576 Schematic Design Guidelines AN-606 for detailed power supply and power sharing recommendations.

Table 4 MSR576 power delivery requirements

S. No.	Power Supply Domain	Nominal DC Voltage (V)	DC Tolerance	Max AC Ripple at BGA balls (mV p-p)	Recommended Ztarget[1] at BGA balls (mΩ)
1	VDDA_SDS	1.1	±5%	10	250
2	VDD_SDS	1.0	±5%	15	100
3	VDDHV_SDS	1.5	±5%	15	400
4	VDD	1.0	±5%	20	50
6	VDDHV	1.5	±5%	25	TBD

1. Fmax = 100 MHz

Considerations for Next Generation Design

The maximum serial bit rate of the MSR576 device is 10.3125 Gbps. The next-generation product will have the same ball-out as MSR576, but the maximum serial bit rate will be 12.5 Gbps. In order to design a board that will have good signal integrity for both devices, the following guidelines are probably sufficient:

- When this document describes a guideline that applies at a frequency that is proportional to the bit rate, design the board to meet that guideline for the bit rate of both MSR576 and the next-generation device. For example, the crosstalk requirement in “Loss Requirements” is < -36 dB at 5.15 GHz, which is 1/2 of 10.3125 Gbps. You should design the board so that crosstalk is < -36 dB at both 5.15 GHz and 6.25 GHz.
- The geometrical guidelines for MSR576, such as the requirement in “Loss Requirements” to match the trace lengths in a differential pair to within +/-10 mils, are sufficient for the next-generation device.
- The next generation device will have different supply voltages, although the pinouts are compatible, so the power supply sections should be designed to easily convert from one set of supply voltages to the other and to supply the current requirements for either device.
- Errata for the MSR576 device should be consulted to identify any potential conflicts between MSR576 and the next generation device.

Board Compliance

Customer Board Compliance

Following are customer board compliance recommendations. Customers are encouraged to have all or subset of these board and packages available. Using these boards and packages can quickly establish if the board and packages meet the design guidelines.

Board Compliance Check

- Measure board S-parameters from 10 MHz to 16+ GHz.
- Insert measure channels into a compliance simulation (see “Customer Board Specific Requirements” on page 7).
- Blocks not available for measurements should be included in a simulation model, and the insertion, return loss and cross talk extrapolated.

Package Compliance Check

- Have blank packages with BGA balls available, where feasible.
- Measure package S-parameters from 10 MHz to 16+ GHz.

Assembled Board Compliance Check

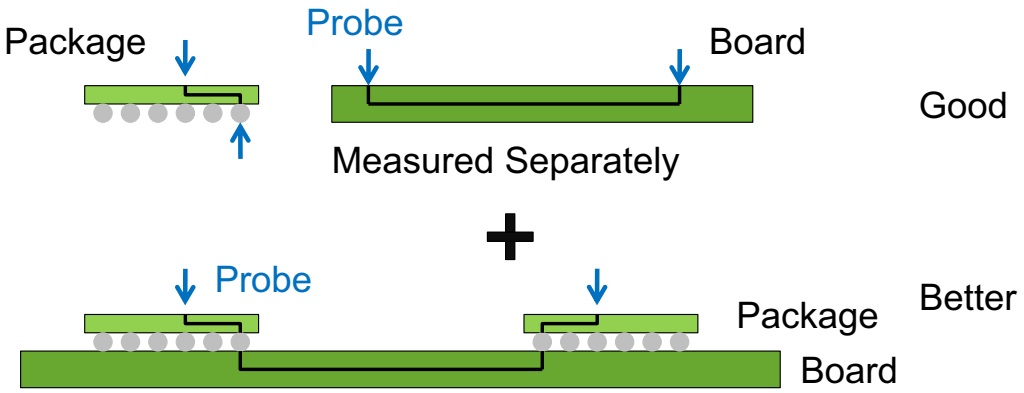
- Mount package(s) on board, and measure the S-parameters of representative channels.
- If a socket is required, it should be measured in the channel.

Compliance Board Setup

Compliance board setup recommendations include:

- Four port differential measurements are recommended.
- Insertion and Return loss, and cross talk should be measured.
- Individual component s-parameter measurements are required. Some may be obtained from the vendors, or other emulation done.
- An assembled board setup is recommended in addition to individual measurements, provided the components are available from vendors. This captures the transitions.

Figure 18 Compliance board setup



Version History

Date	Version	Changes
July 2011	0.1	Initial release.
July 2012	0.2	Grouped layout guidelines together, grouped design and verification guidelines together, updated miscellaneous signal routing section. Updated miscellaneous signal requirements and reference design kit information. Removed power sharing information and put it in the AN-606 document.

7/16/12

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